Remarks

Reconsideration of this Application is respectfully requested.

Claims 12-30 are pending in the application, with claims 12, 18 and 24 being the independent claims.

Based on the following Remarks, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding objections and rejections.

Rejections under the judicially created doctrine of obvious-type double patenting

At paragraph 3 of the Office Action, the Examiner rejected claims 12-30 under the judicially created doctrine of obvious-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 5,497,499 to Garg *et al.* and claims 1-19 of U.S. Patent No. 5,737,624 to Garg *et al.* Applicants obviate the obviousness-type double patenting rejections based upon the terminal disclaimer submitted herewith. Please note that the assignment by the inventors to S-MOS Systems, Inc. was filed in Appl. No. 07/860,719. U.S. Patent No. 5,497,499 issued from Appl. No. 08/219,425, which is a continuation of Appl. No. 07/860,719. U.S. Patent No. 5,737,624 issued from Appl. No. 08/594,401, which is a continuation of Appl. No. 08/219,425.

Rejections under 35 U.S.C. § 102(e)

At paragraph 6 of the Office Action, the Examiner rejected claims 12-30 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,448,705 to Nguyen *et al.*

(hereinafter Nguyen). As set forth below, Applicants submit that Nguyen is not prior art under 35 U.S.C. § 102(e) because "one's own invention whatever the form of disclosure to the public, may not be prior art against oneself, absent a statutory bar." *In re* Facius, 408 F.2d 1396, 1406.

First, Applicants note that the inventors in both the present application and the Nguyen patent were included as part of the S-MOS "Seabird" project team. The S-MOS "Seabird" project team designed the microprocessor architecture that is described in the Nguyen patent. The Nguyen patent describes and claims in part a method of operation in the overall "Seabird" microprocessor architecture.

As part of the "Seabird" project team, Applicants were responsible for the design of the Instruction Execution Unit (IEU). The Applicants' IEU design is described generally in the Nguyen patent. The present application further describes the IEU, initially disclosed in Nguyen, in greater detail to support the invention as claimed in the present application. Thus, the IEU disclosed in the Nguyen patent is derived from the Applicants rather than the inventors listed on the Nguyen patent. The supporting declarations filed herewith set forth the facts as detailed above.[1] Applicants submit that these declarations provide a "satisfactory showing which would lead to a reasonable conclusion" that Applicants are the inventors of the claimed subject matter. *See* MPEP § 716.10 and *In re* Katz, 687 F.2d 450, 455, 215 USPQ 14, 18 (CCPA 1982). For these reasons, Applicants request that the outstanding rejection of claims 12-30 under 35 U.S.C. § 102(e) be withdrawn.

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[1] Filed herewith are true copies of original, signed declarations of Keven Iadonato, Le Nguyen and Sanjiv Garg, which were filed in Appl. No. 08/594,401, now U.S. Patent No. 5,737,624. The declaration of the remaining inventor, Johannes Wang, has not yet been returned.

Rejections under 35 U.S.C. § 102(b)

At paragraph 7 of the Office Action, the Examiner rejected claims 12, 18 and 24 under 35 U.S.C. § 102(b) as being anticipated by Keller, "Look Ahead Processors" (hereinafter Keller). Applicant respectfully traverses these rejections.

Keller appears to describe, at a high level, a register renaming technique for look-ahead processors. According to this technique, registers specified in instructions are denoted by register names. Physical register spaces are each identified by a unique index value. A mapping table is used to link each register name with the index of a physical register which with the register name is currently associated. When an operation involving a given register name issues, the mapping table is accessed and the register name is translated into the index of the physical register with which it is currently associated. Henceforth, the operation addresses this register through its physical index.

According to Keller, each instruction may write to a plurality of different physical destination registers. Consequently, the method described in Keller requires extra functionality to avoid the overwriting of physical registers that may store values required for other currently pending operations. As described in Keller, when an out-of-order operation specifies the same destination (i.e., range) register name as a previous instruction in the instruction sequence, a new physical register must be assigned to the register name. The mapping table must then be updated accordingly in order to avoid overwriting the value in the former physical register. (Keller at 192). Furthermore, the former physical register must be rendered inaccessible to future instructions in order to protect the value stored therein. To determine when a physical register may be reassigned, Keller teaches that a count must

be maintained for each physical register, indicating how may operations have been issued that will reference its value. As each reference occurs, the count is decremented, and the register is made available for reassignment when the count reaches zero. (Keller at 192).

The register renaming technique in Keller is very different from Applicants' invention as claimed. Unlike the method described in Keller, Applicants' claimed invention maintains an association between each instruction in an instruction window and a temporary register, such that each instruction is assigned a temporary storage location as a destination register. As recited in claim 12, Applicants' invention includes, in part:

> a temporary buffer comprising a plurality of storage locations for storing execution results, wherein an execution result for an instruction in an instruction window is stored at one of said plurality of storage locations, said one of said plurality of storage locations being assigned to said instruction in said instruction window.

Because Applicant's invention as claimed assigns a temporary storage location to each instruction, there is no potential for overwriting output values from previously executed instructions. Thus, Applicants' invention as claimed does not require the extra functionality described in Keller for avoiding such overwriting. In particular, Applicants' claimed invention does not require the scoreboarding scheme described in Keller for determining when a particular register may be accessed for reassignment.

Keller does not disclose maintaining an association between each instruction in the instruction window and the temporary register to which an output of each instruction is stored as recited in claim 12. Rather, Keller only maintains an association (via the mapping table) between logical register names and the indices of the physical registers to which they are

currently assigned. Accordingly, Keller fails to anticipate Applicants' claim 12. Thus, Applicants respectfully request that the rejection of claim 12 be reconsidered and withdrawn.

Independent claim 18 is a system claim that, like claim 12, recites an association between each instruction in an instruction window and a temporary register, such that "an execution result for an instruction in an instruction window is stored at one of said plurality of storage locations, said one of said plurality of storage locations being assigned to said instruction in said instruction window." Therefore, for at least this reason, claim 18 is also patentable over Keller. Accordingly, Applicants respectfully request that the rejection of claim 18 also be considered and withdrawn.

Independent claim 24 is a method claim that, like claim 12, recites an association between each instruction in an instruction and a temporary register, in which out-of-order execution results are stored "in storage locations assigned to instructions in an instruction window." Therefore, for at least this reason, claim 24 is also patentable over Keller. Accordingly, Applicants respectfully request that the rejection of claim 24 also be considered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant(s) therefore respectfully request(s) that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn.

It is believed that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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